



Waylon Peters

SoC Engineering Architect, Subsystem Architecture

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SUMMARY

SoC and **subsystem architecture** leader with 18 years of semiconductor experience across RTL design, **IP integration**, platform architecture, **verification** strategy, and production silicon delivery. Converts product requirements into implementable specifications that balance performance, power, area, security, firmware needs, and physical design constraints. Leads architecture exploration, IP selection, subsystem modeling, simulation, protocol analysis, verification planning, **silicon bring up**, debug, and performance characterization. Deep experience with Verilog, SystemVerilog, AMBA AXI, APB, CHI, DDR, PCIe, Ethernet, USB, UFS, SystemVerilog UVM, BFM, synthesis, lint, CDC, low power design, and PPA analysis. Aligns hardware, firmware, software, design verification, and physical design teams while mentoring engineers and reducing integration risk across AI, automotive, networking, and connected device platforms.

EXPERIENCE

Principal SoC Architect, Platform Subsystems

VertexCore Microelectronics 📅 July 2022 to Present 📍 Austin, TX

Owns architecture for compute, memory, interconnect, PCIe, security, and power managed subsystems. Translates enterprise requirements into specifications, validation plans, PPA tradeoffs, and production readiness decisions while coordinating hardware, firmware, software, verification, and **physical design** teams.

- Translated product requirements into subsystem **specifications**, acceptance criteria, and implementation plans.
- Modeled AXI, CHI, APB, DDR, and PCIe dataflows for integration risk reviews.
- Directed UVM validation planning for protocol behavior, performance corners, and **power** states.
- Resolved silicon readiness issues through **simulation**, protocol debug, and cross team reviews.
- Guided architecture decisions balancing **performance**, power, area, **security**, and firmware needs.
- Mentored engineers through design reviews, documentation standards, and integration risk reduction.

Senior SoC Architect, Automotive Compute

Ardent Logic Systems 📅 March 2018 to June 2022 📍 Raleigh, NC

Led automotive compute and edge AI architecture for interconnect and memory subsystems. Coordinated RTL, design verification, firmware, software, synthesis, and physical design contributors through architecture definition, implementation, validation, and release readiness.

- Architected automotive compute and edge AI memory paths with DDR and **PCIe interfaces**.
- Used **synthesis**, lint, CDC, and low power flows to expose implementation risks early.
- Defined verification requirements for protocol compatibility, performance corners, and power state transitions.
- Coordinated **RTL**, **firmware**, software, and physical design reviews for production delivery.
- Investigated **Ethernet** and interconnect performance issues through simulation and targeted protocol analysis.
- Mentored engineers on architecture writing, risk review, and practical subsystem integration.

SoC Integration Architect, Application Processors

BluePeak Semiconductor 📅 August 2013 to February 2018 📍 San Jose, CA

Led application processor IP integration and subsystem architecture across communication, peripheral, and memory functions. Produced implementation guidance, integrated interfaces, aligned verification environments, and supported production silicon debug with cross disciplinary teams.

- Integrated **Verilog** and **SystemVerilog** IP through AXI, APB, USB, UFS, and Ethernet interfaces.
- Created BFM based test environments for interoperability checks and integration validation.
- Documented **dataflow**, **firmware expectations**, interface behavior, and implementation requirements.

STRENGTHS

- 🏗 **Architecture translation**
Turned incomplete product needs into implementable specifications, helping teams make clear decisions before RTL work began.
- 👥 **Cross team leadership**
Aligned RTL, verification, firmware, software, and physical design groups when competing constraints threatened delivery.
- 🔧 **Protocol debugging**
Used simulation and interface analysis to isolate difficult AXI, PCIe, DDR, and Ethernet issues during integration.
- ✅ **Verification planning**
Defined practical checks for functionality, performance corners, power states, and interoperability, giving teams clearer closure targets.
- 🎓 **Engineer mentoring**
Shared architecture review habits and debugging methods that helped colleagues approach difficult subsystem decisions with more confidence.

SKILLS

SoC Architecture

Subsystem Architecture

IP Integration Verilog

SystemVerilog RTL Design UVM

BFM AXI CHI APB DDR PCIe

Ethernet Silicon Bring Up

LANGUAGES

English Native

Spanish Intermediate

MY CAREER

0 MONTHS

- Closed integration defects through simulation, debug sessions, and focused verification reviews.
- Supported **silicon bring up** with protocol analysis and **performance characterization** activities.
- Coordinated specialists across architecture, RTL, verification, firmware, and physical design.

Senior RTL Design Engineer, Memory and Peripherals

Northstar Circuits 📅 June 2010 to July 2013 📍 Phoenix, AZ

Designed memory control and high speed peripheral RTL for production SoC programs. Combined SystemVerilog design, simulation, synthesis, lint, and CDC analysis with clear specifications and close coordination across verification and implementation teams.

- Designed SystemVerilog memory control RTL for **AXI** and **APB** connected subsystems.
- Used simulation, synthesis, **lint**, and **CDC** analysis to improve RTL quality before handoff.
- Built protocol checks for interface behavior, reset sequencing, and corner case coverage.
- Partnered with verification engineers on test planning, **debug**, and closure decisions.
- Reviewed implementation tradeoffs affecting timing, power, **area**, and integration risk.
- Supported production readiness through documentation, defect triage, and design reviews.

RTL Design Engineer, Embedded Communications

MesaWave Technologies 📅 June 2008 to May 2010 📍 Tempe, AZ

Developed embedded SoC peripheral and communication RTL for early production platforms. Built practical design and testbench solutions, supported interface validation, and collaborated with senior engineers on lint, CDC, and release activities.

- Developed Verilog peripheral RTL connected through APB and internal FIFO structures.
- Built testbenches for **communication** paths, reset behavior, and basic protocol validation.
- Applied lint and CDC analysis before design reviews and implementation handoff.
- Debugged simulation failures with waveform analysis and focused reproduction cases.
- Documented interface behavior and test expectations for verification partners.
- Supported release readiness through defect tracking, reviews, and integration assistance.

PROJECTS

Edge AI Interconnect Analysis 📅 2022

Compared interconnect dataflows, memory access patterns, and protocol behavior for an edge AI subsystem, producing architecture guidance for performance, power, area, and firmware coordination.

Automotive Memory Subsystem 📅 2020

Defined a production focused memory subsystem concept using DDR, AXI, CDC, low power analysis, and verification planning for automotive compute requirements.

High Speed Peripheral Integration 📅 2016

Integrated USB, UFS, Ethernet, and APB connected IP with BFM based validation, interface documentation, and targeted protocol debug.

LEADERSHIP & AWARDS

- Technical leadership recognition for production SoC architecture and cross functional delivery, 2024.
- Architecture contribution award for reducing subsystem integration risk across automotive compute programs, 2021.
- Mentor recognition for supporting engineers through design reviews and verification planning, 2023.

EDUCATION

Master of Science in Electrical Engineering

Arizona State University 🎓 GPA: 4.0 📅 2008 📍 Tempe, AZ

Coursework: Digital systems, computer architecture, semiconductor design, integrated circuit design

Bachelor of Science in Computer Engineering

University of Arizona 🎓 GPA: 4.0 📅 2006 📍 Tucson, AZ

Coursework: Computer architecture, digital logic, embedded systems, hardware design

CERTIFICATIONS

- Cadence SystemVerilog and UVM Advanced Verification Training 📅 2024
- Siemens EDA CDC and RTL Quality Workshop 📅 2023

TECHNICAL SKILLS

- **RTL Design:** Verilog, SystemVerilog, RTL
- **Verification:** UVM, BFM, testbenches
- **AMBA Protocols:** AXI, APB, CHI
- **Memory Interfaces:** DDR, memory controllers, dataflow
- **High Speed Interfaces:** PCIe, Ethernet, USB
- **Storage Interfaces:** UFS, firmware interfaces, protocol debug
- **Design Quality:** Synthesis, lint, CDC
- **Low Power Design:** Power states, power intent, PPA analysis
- **Architecture Methods:** IP selection, subsystem modeling, simulation
- **Silicon Delivery:** Silicon bring up, debug, performance characterization

PROFESSIONAL AFFILIATIONS

- Technical Mentor, Semiconductor Architecture Mentoring Circle, 2021 to Present.
- Technical Program Volunteer, IEEE Solid State Circuits community, 2019 to Present.

ADDITIONAL INFORMATION

Work Status : Authorized to work in United States. No sponsorship required.

REFERENCES

AVAILABLE ON REQUEST