



Ariya Harmon

SoC Validation Engineer

☎ (512) 555-6841 ✉ ariya.harmon@example.com

🌐 linkedin.com/example/ariyaharmon 📍 Round Rock, TX 78664

STRENGTHS



Evidence driven testing

Repeated a difficult hardware condition until setup details became clear, giving design partners usable evidence for review.



Issue triage

When findings competed for attention, separated release risks from retest needs and helped engineers focus quickly.



Validation organization

Kept bench records orderly across changing builds, so teammates could find conditions and results without guesswork.



Cross functional work

Shared concise status with hardware stakeholders, and peers began seeking input on difficult validation handoffs.



Junior engineer guidance

Explained repeatable practices through real test examples, helping newer engineers document defects with greater clarity.

SKILLS

SoC validation Hardware validation

Validation planning

Bench validation

Regression testing

Defect reproduction Issue triage

Validation documentation

Hardware development

SUMMARY

Hardware validation professional with six years of progressive experience supporting **system on chip validation** across semiconductor development environments. Career growth includes supervised bench execution, structured validation planning, regression coordination, defect investigation, and milestone readiness support. Builds clear evidence around observed behavior, reproduces failures through controlled conditions, and converts findings into actionable engineering records. Coordinates coverage across **hardware samples** and **development builds** while keeping test results, open findings, retest needs, and release impacts visible to engineering stakeholders. Guides junior engineers on repeatable practices and concise defect documentation. Brings practical judgment, disciplined problem solving, and clear technical communication to **hardware engineering** teams. Ready to contribute reliable validation execution, organized evidence, and thoughtful issue triage within a system on chip development program.

EXPERIENCE

Senior SoC Validation Engineer

Blue Mesa Semiconductor 📅 February 2024 - Present 📍 Austin, TX

Owns SoC validation execution across development milestones, hardware samples, bench activities, regression coverage, issue triage, and release readiness. Guides junior engineers and coordinates evidence with **hardware engineering** stakeholders.

- Translated approved SoC objectives into organized bench activities and traceable validation results.
- Coordinated coverage across **hardware samples** and builds, supporting milestone readiness discussions with clear records.
- Investigated observed SoC behavior through repeatable conditions, narrowing failure scenarios for design review.
- Maintained status summaries covering completed checks, open findings, retests, and release impacts.
- Guided junior engineers on reproducible validation practices and defect documentation for changing configurations.
- Prioritized **validation** findings with hardware stakeholders, grounding milestone decisions in documented results.

SoC Validation Engineer

Trinity Circuit Systems 📅 June 2022 - January 2024 📍 Cedar Park, TX

Executed planned SoC validation across development cycles, with ownership of controlled reproduction, regression comparison, evidence management, and technical handoffs. Protected repeatability while balancing multiple weekly engineering priorities.

- Executed planned SoC validation activities, recording conditions and outcomes for technical review.
- Reproduced hardware issues through controlled sequences, giving development teams focused investigation evidence.
- Organized regression runs after changes, separating recurring behavior from newly introduced issues.
- Prepared milestone documentation that kept test evidence and open findings accessible to stakeholders.
- Managed weekly validation priorities while preserving repeatability and accurate reporting.
- Strengthened issue handoffs with setup context, reproduction steps, results, and retest outcomes.

Hardware Validation Engineer

Hill Country Microelectronics 📅 October 2020 - May 2022 📍 Georgetown, TX

Technical reporting

Cross functional communication

Test execution

Failure investigation

Milestone readiness

Technical status

LANGUAGES

English Native

Spanish Intermediate

MY CAREER



● Senior SoC Validation Engineer at Blue Mesa Semiconductor (2.7 Years)

● SoC Validation Engineer at Trinity Circuit Systems (1.6 Years)

● Hardware Validation Engineer at Hill Country Microelectronics (1.6 Years)

● Junior Hardware Validation Engineer at Central Texas Hardware Lab (11 Months)

Supported integrated hardware validation during SoC development, preparing bench configurations, maintaining reproducible records, tracking defects, and comparing outcomes across hardware revisions. Contributed clear status updates while developing independent troubleshooting judgment.

- Supported integrated hardware validation by following procedures and documenting observed behavior.
- Prepared bench configurations and orderly records so other engineers could reproduce results.
- Logged defects with technical context for triage and tracked retest status through fixes.
- Compared outcomes across hardware revisions, identifying behavior changes requiring further investigation.
- Contributed status updates covering completed validation, active issues, and upcoming test needs.
- Escalated findings requiring deeper design expertise while building independent troubleshooting judgment.

Junior Hardware Validation Engineer

Central Texas Hardware Lab 📅 October 2019 - September 2020 📍 San Marcos, TX

Performed supervised hardware validation procedures, prepared repeatable setups, captured unexpected behavior, and maintained records supporting senior engineering review. Built foundational SoC validation, technical communication, and problem solving capability.

- Executed supervised hardware validation procedures against defined engineering expectations.
- Prepared test setups and verified configuration details before repeatable validation sequences.
- Captured unexpected behavior in structured notes, preserving conditions for senior engineer reproduction.
- Repeated tests after configuration changes and documented whether issues remained present.
- Maintained organized validation records supporting review of completed work and outstanding checks.
- Built foundational SoC validation experience through supervised testing and technical communication.

PROJECTS

SoC Milestone Validation Coverage 📅 2026

Coordinated validation coverage across hardware samples and development builds, connecting bench evidence with milestone readiness decisions. Organized results, unresolved findings, retest needs, and release impacts for engineering review.

Hardware Failure Reproduction Study 📅 2024

Structured repeatable test conditions for observed hardware behavior, captured reproduction evidence, and narrowed failure scenarios for focused design review and issue triage.

LEADERSHIP & AWARDS

- Received senior recognition for clear SoC validation evidence supporting milestone readiness reviews.
- Selected to guide junior engineers on repeatable testing and concise defect documentation.
- Recognized by engineering peers for dependable issue handoffs and organized regression reporting.

EDUCATION

Bachelor's Degree in Electrical Engineering

Texas State University 🎓 GPA: 3.5 📅 2019 📍 San Marcos, TX

Coursework: Circuit Analysis, Digital Systems, Embedded Systems, Electronics Laboratory

CERTIFICATIONS

- SoC Validation Methods Certificate 📅 2024
- Hardware Testing and Debug Certificate 📅 2022

TECHNICAL SKILLS

- **Validation Methods:** SoC validation, Hardware validation, Bench validation
- **Testing Practices:** Regression testing, Test execution, Reproducible testing
- **Defect Management:** Defect reproduction, Issue triage, Retest tracking
- **Technical Records:** Validation documentation, Test records, Technical reporting
- **Hardware Development:** Hardware samples, Development builds, Hardware revisions
- **Failure Analysis:** Failure investigation, Behavior comparison, Evidence capture
- **Release Readiness:** Milestone reviews, Release impact, Readiness tracking
- **Engineering Collaboration:** Design review, Stakeholder communication, Cross functional coordination
- **Bench Operations:** Test setups, Configuration checks, Controlled sequences
- **Team Development:** Junior engineer guidance, Knowledge sharing, Peer review

PROFESSIONAL AFFILIATIONS

- Semiconductor validation community participant, sharing practical methods for reproducible bench testing.
- Electrical engineering alumni participant, supporting conversations about hardware testing careers.

ADDITIONAL INFORMATION

Work Status : Authorized to work in United States. No sponsorship required.

REFERENCES

AVAILABLE ON REQUEST