

Edward Peterson

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SUMMARY

Senior FPGA and **hardware assisted verification** application engineer with 12 years across SoC validation, **FPGA prototyping**, emulation, ASIC verification, and customer facing solution engineering. Translates **RTL to hardware** challenges into practical discovery plans, architecture reviews, evaluations, benchmarks, demonstrations, and proof of concept engagements. Hands on work spans Verilog, VHDL, synthesis, partitioning, clock domains, **hardware bring up**, debug, Xilinx and Intel FPGA architectures, ZeBu, HAPS, and ProtoCompiler workflows. Leads customer site deployments, technical presentations, competitive comparisons, and sales partnership through complex opportunities. Builds trust with architects, engineers, program leaders, and executives by connecting implementation tradeoffs with measurable outcomes. Field findings have informed product and R&D priorities. This background supports clear technical guidance, disciplined opportunity execution, and reliable adoption of hardware assisted verification platforms.

EXPERIENCE

Principal Applications Engineer, FPGA Prototyping

January 2023 - Present

Aperture Logic Systems

San Jose, CA

Leads concurrent pre sales evaluations for large SoC and AI accelerator designs, shaping FPGA prototyping plans, customer deployments, benchmark methods, and field feedback for product teams.

- Converted RTL, partitioning, performance, and debug constraints into executable FPGA prototyping plans.
- Architected HAPS and **ProtoCompiler proof of concept** environments with measurable benchmark criteria.
- Reviewed **clock domains**, memory, interfaces, synthesis constraints, and implementation tradeoffs with **customer architects**.
- Guided customer site configuration, RTL preparation, compile strategy, **hardware bring up**, and debug.
- Partnered with account teams on qualification, milestones, objections, **competitive positioning**, and opportunity execution.
- Presented field findings to R&D, informing scalability, debug, and integration priorities.

Senior Applications Engineer, Hardware Assisted Verification

July 2020 - December 2022

Orion Emulation Technologies

Santa Clara, CA

Directed customer evaluations for **hardware assisted verification** platforms supporting processor, networking, GPU, and custom SoC programs, linking technical evidence with adoption and sales strategy.

- Directed processor, networking, GPU, and custom **SoC** platform evaluations for engineering customers.
- Built RTL through synthesis, **partitioning**, configuration, bring up, and benchmark **proof of concept** flows.
- Diagnosed clocking, partition boundary, RTL assumption, and integration failures during prototype execution.
- Demonstrated engineering debug, prototype value, and schedule risk findings for **program leaders**.
- Supported sales planning with qualification, competitive analysis, milestone tracking, and platform fit recommendations.
- Advised **architects** after evaluations as designs grew in capacity and complexity.

FPGA Prototyping Engineer, SoC Validation

June 2017 - June 2020

NexCore Semiconductor Solutions

Fremont, CA

Developed FPGA prototypes for ASIC and SoC subsystems, balancing implementation constraints, reusable verification flows, benchmark evidence, and clear communication with technical leaders.

- Developed ASIC and SoC FPGA prototypes using **Verilog** and VHDL on Xilinx and Intel architectures.
- Created multi **FPGA** partitioning strategies balancing resources, timing, interconnect capacity, and debug access.
- Performed **hardware bring up** and root cause **debug** across RTL, clocks, interfaces, and transactors.
- Integrated simulation and FPGA workflows so verification teams reused test environments for hardware validation.
- Produced **benchmarks** comparing compile behavior, runtime **performance**, capacity, and debug workflows.
- Presented architecture limits and validation results to design, verification, and software leaders.

ASIC Verification Engineer, RTL Validation

June 2014 - May 2017

Vertex Microelectronics Lab

Milpitas, CA

Verified RTL blocks and SoC subsystems while preparing synthesizable designs for FPGA validation, connecting simulation evidence with implementation decisions and risk reduction.

- Verified **RTL** blocks and SoC subsystems through Verilog test environments and simulation.
- Analyzed waveforms, assertions, and defects to isolate design risks before implementation.
- Prepared synthesizable RTL subsets for FPGA validation and hardware implementation review.

- Investigated clock domain and reset issues using RTL and simulation evidence.
- Supported prototype builds through interface checks, bring up tests, and debug documentation.
- Evaluated **synthesis** reports and **FPGA** resource utilization to identify implementation bottlenecks.

PROJECTS

AI Accelerator FPGA Evaluation 📅 2024

Built a customer evaluation plan for an AI accelerator design, connecting RTL preparation, partitioning, ProtoCompiler execution, benchmark criteria, and executive review around practical adoption decisions.

Multi FPGA SoC Prototype 📅 2021

Created a multi FPGA prototype workflow for a complex SoC, linking synthesis, clock analysis, hardware bring up, debug access, and reusable simulation environments.

LEADERSHIP & AWARDS

- Advanced FPGA Design and Verification Certificate, University Continuing Education, 2021.
- Hardware Verification Technical Mentoring Circle, Mentor, 2022 - Present.
- Recognized by customer engineering teams for clear evaluation guidance and practical prototype debug support.

EDUCATION

Bachelor's Degree in Computer Engineering

2014

San Jose State University GPA: 3.8

San Jose, CA

Coursework: Digital systems, computer architecture, embedded systems, hardware design

CERTIFICATIONS

- Advanced FPGA Design and Verification Certificate 📅 2021
- Bachelor of Science in Computer Engineering 📅 2014

TECHNICAL SKILLS

- **FPGA Platforms:** HAPS, Xilinx FPGA, Intel FPGA
- **Emulation Platforms:** ZeBu 200, ZS5 Emulation, hardware emulation
- **RTL Languages:** Verilog, VHDL, synthesizable RTL
- **Compilation Tools:** ProtoCompiler, synthesis, compile strategy
- **Validation Methods:** SoC validation, ASIC verification, simulation
- **Prototype Architecture:** partitioning, clock domains, interfaces
- **Hardware Bring Up:** bring up tests, transactors, board debug
- **Debug Analysis:** waveform analysis, assertions, root cause analysis
- **Evaluation Methods:** proof of concept, benchmarking, technical evaluation
- **Customer Engineering:** technical discovery, architecture reviews, demonstrations
- **Sales Engineering:** pre sales engineering, opportunity qualification, competitive positioning
- **Presentation Skills:** technical presentations, executive briefings, objection handling

SKILLS

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|----------------------------------|---------------------|-----------------|-------------|
| • FPGA Prototyping | • ASIC Verification | • HAPS | • Verilog |
| • Hardware Assisted Verification | • RTL Workflows | • ProtoCompiler | • VHDL |
| • Emulation | • ZeBu 200 | • Xilinx FPGA | • Synthesis |
| • SoC Validation | • ZS5 Emulation | • Intel FPGA | |

PROFESSIONAL AFFILIATIONS

- Hardware Verification Technical Mentoring Circle, Mentor, 2022 - Present.
- Silicon Prototyping Technical Forum, Member, 2019 - Present.

LANGUAGES

- English (Native)
- Spanish (Intermediate)

ADDITIONAL INFORMATION

Work Status : Authorized to work in United States. No sponsorship required.

REFERENCES

AVAILABLE ON REQUEST