



Camden Ramsey

Sr. Staff R&D Engineer, Electromagnetic Methodology

☎ (603) 555-7319 ✉ camden.ramsey@example.com

🌐 linkedin.com/example/camdenramsey 📍 Nashua, NH 03060

STRENGTHS

- 🔧 **Methodology leadership**
Built reusable extraction practices across design teams, and engineers began seeking guidance on difficult solver decisions.
- 🔍 **First principles analysis**
Traced coupling and discontinuity issues back to geometry, ports, and materials, producing changes teams could apply.
- 👥 **Cross team delivery**
Worked across circuit, package, layout, and methodology groups; shared reviews moved issues toward practical closure.
- ♥️ **Simulation correlation**
Connected field solver output with RF SPICE behavior, giving circuit teams greater confidence in extracted models.
- 🎓 **Technical mentoring**
Explained solver tradeoffs through real design examples, helping senior engineers make clearer and faster choices.

SKILLS

- Electromagnetic Theory
- Electromagnetic Extraction
- 3DIC Design High Speed SERDES
- CMOS Technology
- FinFET Technology
- GAA Technology Helic HFSS
- ADS RF SPICE Field Solvers

SUMMARY

Sr. Staff R&D Engineer with 14 years of semiconductor **design enablement** and methodology experience focused on **electromagnetic extraction**, simulation, and **high speed SERDES**. Hands on background spans CMOS, FinFET, and GAA technologies, advanced 3DIC designs, package structures, and interfaces from 10Gbps through 500Gbps. Develops practical Helic, HFSS, ADS, and RF SPICE flows that connect field solver results with circuit behavior and production design decisions. Leads **globally distributed teams** through electromagnetic integrity investigations, model integration, correlation, and solution deployment across product lines. Partners with circuit, package, layout, and methodology experts to resolve coupling, return path, discontinuity, parasitic, and convergence issues. Combines technical depth, mentoring, and clear communication to improve performance, reliability, and reusable design methodology.

EXPERIENCE

Sr. Staff R&D Engineer, Electromagnetic Methodology

GraniteWave Microelectronics 📅 February 2022 - Present 📍 Nashua, NH

Leads electromagnetic **design methodology** for advanced 3DIC and high speed SERDES programs. Owns extraction, simulation, model usage, correlation, and deployment across multiple silicon teams. Guides senior engineers and aligns circuit, package, layout, and methodology decisions with performance and reliability goals.

- Defined **3DIC** extraction flows for SERDES products operating from 112Gbps through **500Gbps**.
- Qualified **Helic**, **HFSS**, and ADS workflows for interconnect and package analysis.
- Directed field solver investigations that connected electromagnetic results with **RF SPICE** behavior.
- Established port, termination, frequency, convergence, and extracted model usage guidance.
- Resolved cross domain integrity issues with circuit, package, layout, and methodology teams.
- Mentored senior engineers on solver tradeoffs, correlation, extraction accuracy, and deployment.

Staff R&D Engineer, Signal and Electromagnetic Integrity

Pioneer SerDes Labs 📅 January 2018 - January 2022 📍 Boston, MA

Owned electromagnetic analysis and methodology for **high speed SERDES** interconnects across FinFET product generations. Built reusable HFSS and ADS workflows, correlated extracted models with RF SPICE studies, and guided distributed engineering groups through production focused technical reviews.

- Owned electromagnetic analysis for **FinFET** channels spanning 56Gbps through 224Gbps.
- Built HFSS and **ADS** workflows for package and on die structures.
- Investigated coupling, **return path**, **discontinuity**, and parasitic effects from first principles.
- Integrated extracted models into circuit simulations with physical design partners.
- Created criteria for **ports**, meshing, frequency coverage, and model quality.
- Deployed validated analysis flows across distributed engineering groups before production milestones.

Senior R&D Engineer, High Speed Interconnect

Seacoast Integrated Circuits 📅 June 2015 - December 2017 📍 Portsmouth, NH

Developed **electromagnetic extraction** methods for CMOS and early FinFET interconnects supporting SERDES development and package integration. Applied **field solvers** and RF SPICE to evaluate transmission structures, model behavior, design margins, and practical geometry changes.

- Developed extraction approaches for **CMOS** and FinFET SERDES interconnect structures.
- Characterized transmission lines, vias, **coupling**, and package transitions with HFSS and ADS.
- Ran **RF SPICE** studies using extracted models for circuit level evaluation.
- Identified geometry changes when electromagnetic effects threatened interface margins.
- Compared solver settings against reference structures and documented methodology limits.

Signal Integrity Model Integration

Design Enablement

LANGUAGES

English Native

Spanish Intermediate

MY CAREER



● Sr. Staff R&D Engineer, Electromagnetic Methodology at GraniteWave Microelectronics (4.7 Years)

● Staff R&D Engineer, Signal and Electromagnetic Integrity at Pioneer SerDes Labs (4 Years)

● Senior R&D Engineer, High Speed Interconnect at Seacoast Integrated Circuits (2.5 Years)

● R&D Engineer, Electromagnetic Extraction at Atlas Semiconductor Research (2.8 Years)

- Presented reusable analysis examples during circuit, layout, and package design reviews.

R&D Engineer, Electromagnetic Extraction

Atlas Semiconductor Research 📅 August 2012 - May 2015 📍 Albany, NY

Supported **electromagnetic extraction** and simulation research for CMOS high speed designs. Created interconnect structures, connected ADS and RF SPICE studies with extracted models, investigated setup discrepancies, and documented repeatable procedures for senior methodology engineers.

- Created field solver structures for transmission lines, vias, and coupled **interconnects**.
- Evaluated electromagnetic behavior across **frequency ranges** for CMOS research designs.
- Connected ADS and **RF SPICE** studies with extracted interconnect models.
- Investigated discrepancies across geometry, materials, ports, boundaries, and conversion settings.
- Documented repeatable extraction procedures that improved consistency across research analyses.
- Contributed validated models to cross functional semiconductor design studies.

PROJECTS

500Gbps SERDES Electromagnetic Methodology 📅 2024

Protected signal and electromagnetic integrity across advanced SERDES designs by combining Helic, HFSS, ADS, and RF SPICE methods. Established practical model settings and review guidance for high speed design decisions.

3DIC Extraction Flow Deployment 📅 2023

Connected package, interconnect, and circuit analysis through a reusable 3DIC extraction flow. Improved team alignment through shared criteria for ports, frequency coverage, convergence, correlation, and model quality.

LEADERSHIP & AWARDS

- IEEE Senior Member, recognized in 2021 for sustained technical contribution in electrical engineering.
- Technical Mentor, High Speed Design Methodology Council, guiding engineers through practical extraction and simulation decisions.
- Peer Review Lead, Semiconductor Electromagnetics Working Group, supporting clear technical review and solution deployment.

EDUCATION

Master of Science in Electrical Engineering

Rensselaer Polytechnic Institute 🎓 GPA: 4.0 📅 2012 📍 Troy, NY

Coursework: *Electromagnetic theory, microwave engineering, semiconductor devices, computational methods*

CERTIFICATIONS

- IEEE Senior Member 📅 2021
- IEEE Electromagnetics Society Member 📅 2021

TECHNICAL SKILLS

- **Electromagnetic Solvers:** Helic, HFSS, ADS
- **RF Simulation:** RF SPICE, ADS, extracted models
- **Semiconductor Technologies:** CMOS, FinFET, GAA
- **High Speed Interfaces:** SERDES, 10Gbps, 500Gbps
- **3DIC Design:** 3DIC, package structures, interconnects
- **Field Analysis:** transmission lines, vias, coupled structures
- **Model Development:** ports, terminations, frequency ranges
- **Simulation Quality:** meshing, convergence, model correlation
- **Integrity Analysis:** signal integrity, electromagnetic integrity, parasitics

- **Design Methodology:** extraction flows, simulation flows, design signoff
- **Technical Collaboration:** circuit teams, package teams, layout teams
- **Deployment Practices:** solution deployment, reusable flows, product lines

PROFESSIONAL AFFILIATIONS

- High Speed Design Methodology Council, Technical Mentor, 2022 - Present.
- Semiconductor Electromagnetics Working Group, Peer Review Lead, 2023 - Present.

ADDITIONAL INFORMATION

Work Status : Authorized to work in United States. No sponsorship required.

REFERENCES

AVAILABLE ON REQUEST