# Levi Le

(630) 555-7426 levi.le@example.com
linkedin.com/example/levile Naperville, IL 60540

## SUMMARY

Verification Engineer with seven years validating complex digital hardware for low latency computing, networking, FPGA, ASIC, and acceleration platforms. Builds reusable UVM environments at block and system levels using SystemVerilog, Verilog, C++, Python, shell scripting, Linux, assertions, scoreboards, reference models, and **functional coverage**. Automates regression execution, result tracking, failure classification, reporting, and coverage analysis, giving RTL and **software teams** fast feedback during active development. Career growth includes ownership of verification plans, mentoring junior engineers, coordinating **hardware software validation**, and driving **coverage closure** across distributed teams. Brings practical judgment to test strategy, interface behavior, failure isolation, and production quality. This background supports dependable verification for performance sensitive hardware and complete engineering solutions.

## EXPERIENCE

### Senior Verification Engineer

January 2024 - Present

Vector Harbor Technologies

*Chicago, IL*

Owns verification strategy for latency sensitive FPGA and ASIC subsystems, guiding reusable environments, automation, coverage, debugging, and cross functional delivery.

- Translated architecture specifications into **UVM** plans, assertions, scoreboards, and coverage models for FPGA subsystems.
- Built **SystemVerilog** environments with protocol agents and **C++** references for end to end transaction checking.
- Automated **Python** regressions in **Linux** with seed control, parallel runs, failure classification, and coverage aggregation.
- Debugged waveforms, assertions, transactions, and scoreboards with commercial **EDA tools** before RTL reviews.
- Tracked functional and code coverage gaps, then added targeted tests and constraints before release milestones.
- Coordinated interface changes, firmware interactions, reproducible failures, and priorities across distributed RTL and software teams.

### Verification Engineer

July 2021 - December 2023

Prairie Logic Systems

*Schaumburg, IL*

Developed reusable UVM verification infrastructure for high throughput digital designs, connecting **testbench development**, automation, reference modeling, dashboards, and closure decisions.

- Developed reusable **UVM** agents and block testbenches for stimulus, monitoring, checking, and coverage collection.
- Implemented SystemVerilog **assertions** and **functional coverage** for protocol, reset, backpressure, and error scenarios.
- Created Python and shell automation for regression launches, log parsing, reruns, tracking, and reporting.
- Integrated C++ reference models for transaction comparisons across algorithmic datapaths and control logic.
- Isolated timing, initialization, and state machine defects with **RTL** designers using reproducible failure cases.
- Maintained regression dashboards showing failures and coverage status for evidence based closure decisions.

### Associate Verification Engineer

June 2019 - June 2021

Midwest Silicon Labs

*Aurora, IL*

Supported supervised verification of digital interface blocks, extending UVM components, running Linux regressions, improving triage, and connecting simulation findings with software validation.

- Created directed and constrained random **SystemVerilog** tests for digital interface blocks under senior guidance.
- Extended **UVM** monitors, drivers, sequences, and **scoreboards** for register behavior and protocol corner cases.
- Ran Linux regressions with **third party EDA tools**, reviewing logs and waveforms for failure ownership.
- Wrote Python utilities that normalized regression results and grouped repeated signatures across test seeds.
- Added **functional coverage** points and crosses for configuration modes and error scenarios in verification plans.
- Reproduced interface issues in simulation and documented expected transactions for software integration reviews.

## PROJECTS

### Low Latency Subsystem Verification 2025

Created a reusable verification flow for performance sensitive hardware, combining UVM stimulus, C++ reference behavior, Linux regressions, coverage tracking, and failure reporting. Work connected system behavior with actionable feedback for engineering teams.

### Coverage Closure Reporting Flow 2023

Built a reporting workflow that consolidated regression outcomes, functional coverage, repeated failures, and open gaps. Clear summaries helped engineers select focused tests and make closure decisions with stronger evidence.

## LEADERSHIP & AWARDS

- Selected as verification owner for latency sensitive FPGA and ASIC subsystem delivery, 2024.
- Recognized by engineering leads for reusable UVM infrastructure and dependable regression reporting, 2023.
- Mentored junior verification engineers through testbench development, debugging, and coverage review, 2022.

## EDUCATION

**Bachelor's Degree in Computer Engineering** 2019

University of Illinois Chicago GPA: 0 *Chicago, IL*

***Coursework:*** *Digital logic, computer architecture, operating systems, embedded systems*

## CERTIFICATIONS

- Siemens UVM Fundamentals Training Certificate 2023
- Linux Foundation Introduction to Linux Certificate 2022

## TECHNICAL SKILLS

- **Verification Methodology:** UVM, constrained random verification, metrics based verification
- **Hardware Description Languages:** SystemVerilog, Verilog, assertions
- **Programming Languages:** C++, Python, shell scripting
- **Testbench Architecture:** Block level testbenches, system level testbenches, scoreboards
- **Coverage Analysis:** Functional coverage, code coverage, coverage closure
- **Regression Management:** Regression automation, regression tracking, result reporting
- **Simulation Debugging:** Waveform analysis, failure triage, root cause isolation
- **Hardware Platforms:** ASIC verification, FPGA verification, digital interfaces
- **Operating Systems:** Linux, command line tools, shell environments
- **EDA Software:** Third party EDA tools, simulation tools, debug tools
- **Reference Modeling:** C++ reference models, transaction checking, expected behavior
- **Integration Validation:** Hardware software validation, interface testing, end to end validation

## SKILLS

- UVM
- SystemVerilog
- Verilog
- C++
- Python
- Linux
- Shell scripting
- EDA tools
- RTL verification
- ASIC verification
- FPGA verification
- Testbench development
- Regression automation
- Functional coverage
- Hardware software validation

## PROFESSIONAL AFFILIATIONS

- IEEE Computer Society member, focused on digital design and verification practice.
- Accellera Systems Initiative community participant, following UVM methodology and verification standards.

## LANGUAGES

- English (Native)
- French (Beginner)

## ADDITIONAL INFORMATION

**Work Status** : Authorized to work in United States. No sponsorship required.

## REFERENCES

AVAILABLE ON REQUEST